

# High Speed, Precision, JFET Input Instrumentation Amplifier (Fixed Gain = 10 or 100)

## FEATURES

- Slew Rate: 30V/μs
- Gain-Bandwidth Product: 35MHz
- Settling Time (0.01%): 3μs
- Overdrive Recovery: 0.4μs
- Gain Error: 0.05% Max
- Gain Drift: 5ppm/°C
- Gain Nonlinearity: 16ppm Max
- Offset Voltage (Input + Output): 600μV Max  
– Drift with Temperature: 2μV/°C
- Input Bias Current: 40pA Max
- Input Offset Current: 40pA Max  
– Drift with Temperature (to 70°C): 0.5pA/°C

## APPLICATIONS

- Fast Settling Analog Signal Processing
- Multiplexed Input Data Acquisition Systems
- High Source Impedance Signal Amplification from High Resistance Bridges, Capacitance Sensors, Photodetector Sensors
- Bridge Amplifier with < 1Hz Lowpass Filtering

## DESCRIPTION

The LT<sup>®</sup>1102 is the first fast FET input instrumentation amplifier offered in the low cost, space saving 8-pin packages. Fixed gains of 10 and 100 are provided with excellent gain accuracy (0.01%) and non-linearity (3ppm). No external gain setting resistor is required.

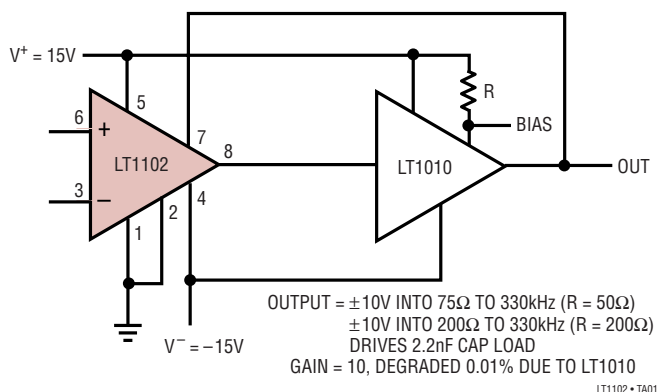
Slew rate, settling time, gain-bandwidth product, overdrive recovery time are all improved compared to competitive high speed instrumentation amplifiers.

Industry best speed performance is combined with impressive precision specifications: less than 10pA input bias and offset currents, 180μV offset voltage. Unlike other FET input instrumentation amplifiers, on the LT1102 there is no output offset voltage contribution to total error, and input bias currents do not double with every 10°C rise in temperature. Indeed, at 70°C ambient temperature the input bias current is only 40pA.

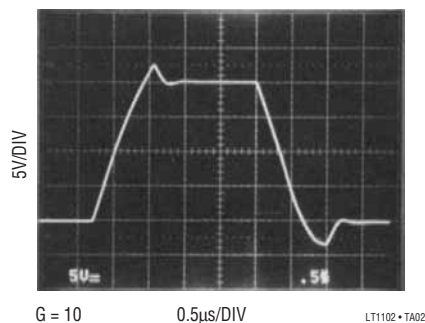
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## TYPICAL APPLICATION

**Wideband Instrumentation Amplifier  
with ±150mA Output Current**



**Slew Rate**



# LT1102

## ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage .....  $\pm 20\text{V}$   
 Differential Input Voltage .....  $\pm 40\text{V}$   
 Input Voltage .....  $\pm 20\text{V}$

Output Short-Circuit Duration ..... Indefinite  
 Operating Temperature Range  
 LT1102I .....  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$   
 LT1102AC/LT1102C .....  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$   
 LT1102AM/LT1102M (**OBSELETE**).....  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$   
 Storage Temperature Range .....  $-65^{\circ}\text{C}$  to  $150^{\circ}\text{C}$   
 Lead Temperature (Soldering, 10 sec) .....  $300^{\circ}\text{C}$

**Order Options** Tape and Reel: Add #TR  
 Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF  
 Lead Free Part Marking: <http://www.linear.com/leadfree/>

## PACKAGE/ORDER INFORMATION

<p>H PACKAGE 8-LEAD TO-5 METAL CAN</p> <p><b>OBSELETE PACKAGE</b> Consider the N8 Package for Alternate Source</p>	<p>ORDER PART NUMBER</p> <p>LT1102AMH LT1102MH LT1102ACH LT1102CH</p>	<p>TOP VIEW LT1102</p> <p>N8 PACKAGE 8-LEAD PDIP <math>T_{JMAX} = 100^{\circ}\text{C}</math>, <math>\theta_{JA} = 130^{\circ}\text{C/W}</math></p> <p>J8 PACKAGE 8-LEAD CERDIP</p> <p><b>OBSELETE PACKAGE</b> Consider the N8 Package for Alternate Source</p>	<p>ORDER PART NUMBER</p> <p>LT1102IN8 LT1102ACN8 LT1102CN8</p> <p>LT1102MJ8 LT1102CJ8</p> <p>LT1102 • P0101</p>
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Consult LTC Marketing for parts specified with wider operating temperature ranges.

**ELECTRICAL CHARACTERISTICS**  $V_S = \pm 15V, V_{CM} = 0V, T_A = 25^\circ C, \text{Gain} = 10 \text{ or } 100, \text{ unless otherwise noted.}$

SYMBOL	PARAMETER	CONDITIONS	LT1102AM/AC			LT1102M/I/C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$G_E$	Gain Error	$V_O = \pm 10V, R_L = 50k \text{ or } 2k$		0.010	0.050		0.012	0.070	%
$G_{NL}$	Gain Nonlinearity	$G = 100, R_L = 50k$		3	14		4	18	ppm
		$G = 100, R_L = 2k$		8	20		8	25	ppm
		$G = 10, R_L = 50k \text{ or } 2k$		7	16		7	30	ppm
$V_{OS}$	Input Offset Voltage		180	600		200	900	$\mu V$	
$I_{OS}$	Input Offset Current		3	40		4	60	$\mu A$	
$I_B$	Input Bias Current		$\pm 3$	$\pm 40$		$\pm 4$	$\pm 60$	$\mu A$	
	Input Resistance Common Mode	$V_{CM} = -11V \text{ to } 8V$		$10^{12}$			$10^{12}$	$\Omega$	
	Differential Mode	$V_{CM} = 8V \text{ to } 11V$		$10^{11}$			$10^{11}$	$\Omega$	
				$10^{12}$			$10^{12}$	$\Omega$	
$e_n$	Input Noise Voltage	0.1Hz to 10Hz		2.8			2.8	$\mu V_{P-P}$	
	Input Noise Voltage Density	$f_0 = 10Hz$		37			37	$nV/\sqrt{Hz}$	
		$f_0 = 1000Hz \text{ (Note 2)}$		19	30		20	$nV/\sqrt{Hz}$	
	Input Noise Current Density	$f_0 = 1000Hz, 10Hz \text{ (Note 3)}$		1.5	4		2	5	$fA/\sqrt{Hz}$
	Input Voltage Range		$\pm 10.5$	$\pm 11.5$		$\pm 10.5$	$\pm 11.5$	V	
CMRR	Common Mode Rejection Ratio	1k Source Imbalance, $V_{CM} = \pm 10.5V$	84	98		82	97	dB	
PSRR	Power Supply Rejection Ratio	$V_S = \pm 9V \text{ to } \pm 18V$	88	102		86	101	dB	
$I_S$	Supply Current		3.3	5.0		3.4	5.6	mA	
$V_O$	Maximum Output Voltage Swing	$R_L = 50k$	$\pm 13.0$	$\pm 13.5$		$\pm 13.0$	$\pm 13.5$	V	
		$R_L = 2k$	$\pm 12.0$	$\pm 13.0$		$\pm 12.0$	$\pm 13.0$	V	
BW	Bandwidth	$G = 100 \text{ (Note 4)}$	120	220		100	220	kHz	
		$G = 10 \text{ (Note 4)}$	2.0	3.5		1.7	3.5	MHz	
SR	Slew Rate	$G = 100, V_{IN} = \pm 0.13V, V_O = \pm 5V$	12	17		10	17	$V/\mu s$	
		$G = 10, V_{IN} = \pm 1V, V_O = \pm 5V$	21	30		18	30	$V/\mu s$	
	Overdrive Recovery	50% Overdrive (Note 5)		400		400	ns		
	Settling Time	$V_O = 20V \text{ Step (Note 4)}$							
		$G = 10 \text{ to } 0.05\%$		1.8	4.0		1.8	4.0	$\mu s$
		$G = 10 \text{ to } 0.01\%$		3.0	6.5		3.0	6.5	$\mu s$
		$G = 100 \text{ to } 0.05\%$		7	13		7	13	$\mu s$
		$G = 100 \text{ to } 0.01\%$		9	18		9	18	$\mu s$

**ELECTRICAL CHARACTERISTICS**  $V_S = \pm 15V$ ,  $V_{CM} = 0V$ , Gain = 10 or 100,  $-55^\circ C \leq T_A \leq 125^\circ C$  for AM/M grades,  $-40^\circ C \leq T_A \leq 85^\circ C$  for I grades, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1102AM			LT1102M/I			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$G_E$	Gain Error	$G = 100, V_O = \pm 10V, R_L = 50k \text{ or } 2k$		0.10	0.25		0.10	0.30	%
		$G = 10, V_O = \pm 10V, R_L = 50k \text{ or } 2k$		0.05	0.12		0.06	0.15	%
$TCG_E$	Gain Error Drift (Note 6)	$G = 100, R_L = 50k \text{ or } 2k$		9	20		10	25	ppm/ $^\circ C$
		$G = 10, R_L = 50k \text{ or } 2k$		5	10		6	14	ppm/ $^\circ C$
$G_{NL}$	Gain Nonlinearity	$G = 100, R_L = 50k$		20	70		24	90	ppm
		$G = 100, R_L = 2k$		28	85		32	110	ppm
		$G = 10, R_L = 50k \text{ or } 2k$		9	20		9	24	ppm
$V_{OS}$	Input Offset Voltage			300	1400		400	2000	$\mu V$
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 6)		2	8		3	12	$\mu V/^\circ C$
$I_{OS}$	Input Offset Current			0.3	4		0.4	6	nA
$I_B$	Input Bias Current			$\pm 2$	$\pm 10$		$\pm 2.5$	$\pm 15$	nA
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10.3V$		82	97		80	96	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V \text{ to } \pm 17V$		88	100		84	99	dB
$I_S$	Supply Current	$T_A = 125^\circ C$		2.5			2.5		mA
$V_O$	Maximal Output Voltage Swing	$R_L = 50k$	$\pm 12.5$	$\pm 13.2$		$\pm 12.5$	$\pm 13.2$		V
		$R_L = 2k$	$\pm 12.0$	$\pm 12.6$		$\pm 12.0$	$\pm 12.6$		V

$V_S = \pm 15V$ ,  $V_{CM} = 0V$ , Gain = 10 or 100,  $0^\circ C \leq T_A \leq 70^\circ C$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1102AC			LT1102C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$G_E$	Gain Error	$G = 100, V_O = \pm 10V, R_L = 50k \text{ or } 2k$		0.04	0.11		0.05	0.14	%
		$G = 10, V_O = \pm 10V, R_L = 50k \text{ or } 2k$		0.03	0.09		0.04	0.12	%
$TCG_E$	Gain Error Drift (Note 6)	$G = 100, R_L = 50k \text{ or } 2k$		8	18		9	22	ppm/ $^\circ C$
		$G = 10, R_L = 50k \text{ or } 2k$		5	10		6	14	ppm/ $^\circ C$
$G_{NL}$	Gain Nonlinearity	$G = 100, R_L = 50k$		8	30		9	40	ppm
		$G = 100, R_L = 2k$		11	36		12	48	ppm
		$G = 10, R_L = 50k \text{ or } 2k$		8	18		8	22	ppm
$V_{OS}$	Input Offset Voltage			230	1000		280	1400	$\mu V$
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 6)		2	8		3	12	$\mu V/^\circ C$
$I_{OS}$	Input Offset Current			10	150		15	220	pA
$\Delta I_{OS}/\Delta T$	Input Offset Current Drift	(Note 6)		0.5	3		0.5	4	pA/ $^\circ C$
$I_B$	Input Bias Current			$\pm 40$	$\pm 300$		$\pm 50$	$\pm 400$	pA
$\Delta I_B/\Delta T$	Input Bias Current Drift	(Note 6)		1	4		1	6	pA/ $^\circ C$
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10.3V$		83	98		81	97	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V \text{ to } \pm 17V$		87	101		85	100	dB
$I_S$	Supply Current	$T_A = 70^\circ C$		2.8			2.9		mA
$V_O$	Maximum Output Voltage Swing	$R_L = 50k$	$\pm 12.8$	$\pm 13.4$		$\pm 12.8$	$\pm 13.4$		V
		$R_L = 2k$	$\pm 12.0$	$\pm 12.8$		$\pm 12.0$	$\pm 12.8$		V

## ELECTRICAL CHARACTERISTICS

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** This parameter is tested on a sample basis only.

**Note 3:** Current noise is calculated from the formula:

$$i_n = (2qI_B)^{1/2}$$

where  $q = 1.6 \cdot 10^{-19}$  coulomb. The noise of source resistors up to  $1G\Omega$  swamps the contribution of current noise.

**Note 4:** This parameter is not tested. It is guaranteed by design and by inference from the slew rate measurement.

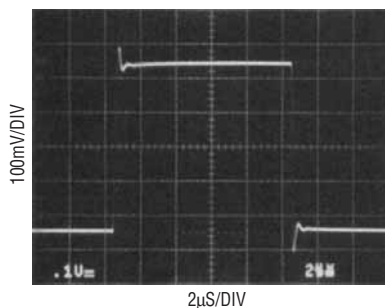
**Note 5:** Overdrive recovery is defined as the time delay from the removal of an input overdrive to the output's return from saturation to linear operation.

50% overdrive equals  $V_{IN} = \pm 2V$  ( $G = 10$ ) or  $V_{IN} = \pm 200mV$  ( $G = 100$ ).

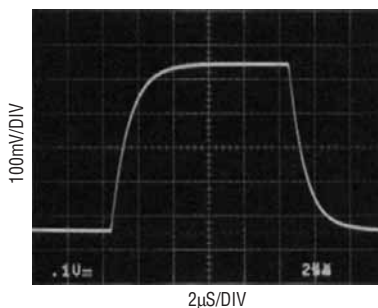
**Note 6:** This parameter is not tested. It is guaranteed by design and by inference from other tests.

## TYPICAL PERFORMANCE CHARACTERISTICS

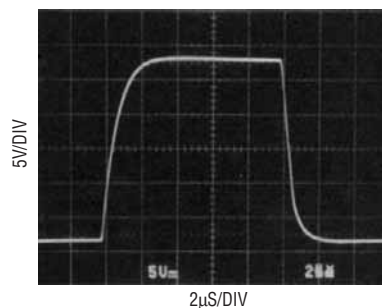
Small Signal Response,  $G = 10$   
(Input = 50mV Pulse)



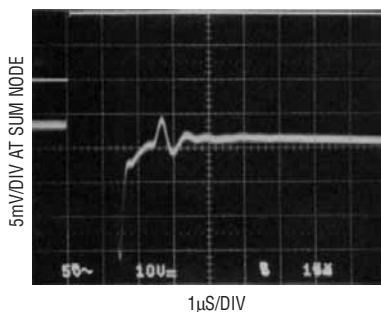
Small Signal Response,  $G = 100$   
(Input = 5mV Pulse)



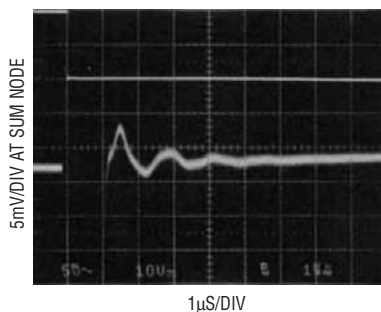
Slew Rate,  $G = 100$   
(Input =  $\pm 130mV$  Pulse)



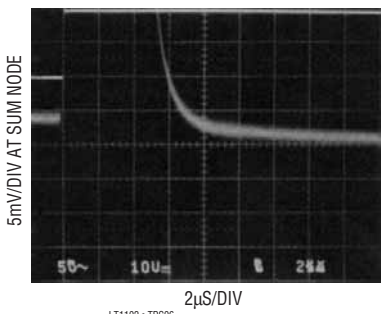
Settling Time,  $G = 10$   
(Input From  $-10V$  to  $10V$ )



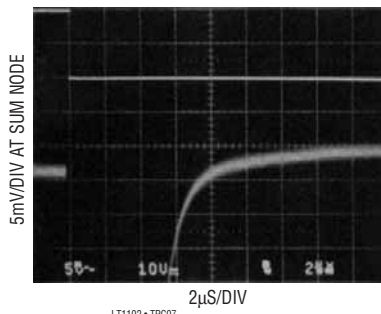
Settling Time,  $G = 10$   
(Input From  $10V$  to  $-10V$ )



Settling Time,  $G = 100$   
(Input From  $-10V$  to  $10V$ )

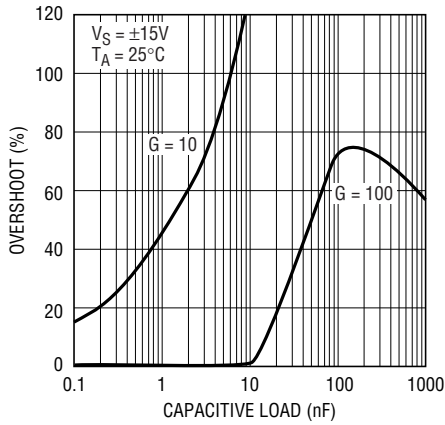


Settling Time,  $G = 100$   
(Input From  $10V$  to  $-10V$ )



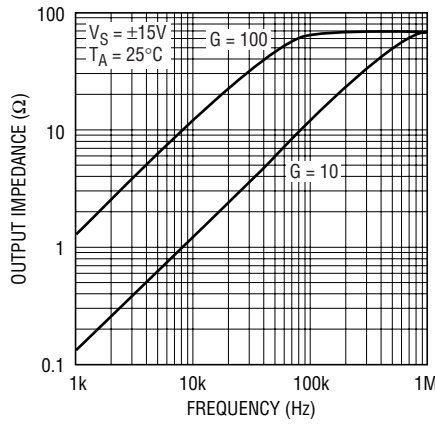
# TYPICAL PERFORMANCE CHARACTERISTICS

**Capacitive Load Handling**



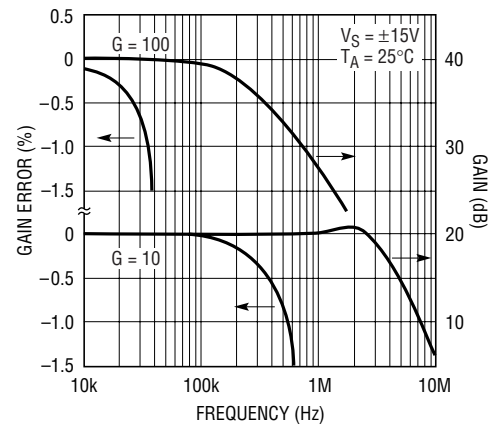
LT1102 • TPC08

**Output Impedance vs Frequency**



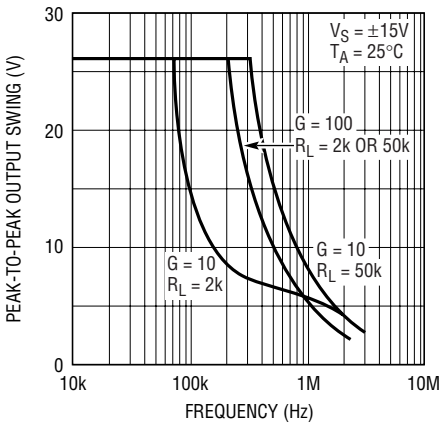
LT1102 • TPC09

**Gain vs Frequency**



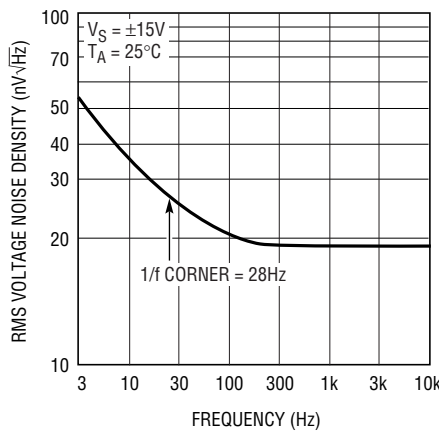
LT1102 • TPC10

**Undistorted Output vs Frequency**



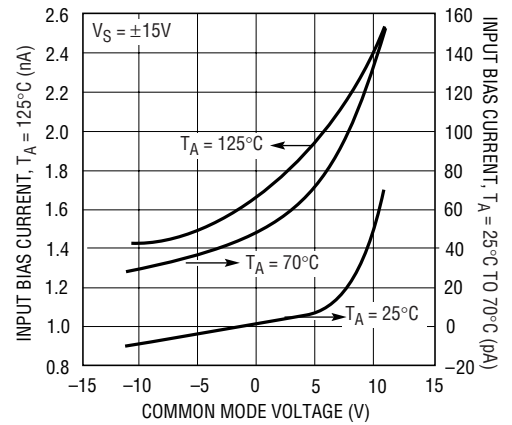
LT1102 • TPC11

**Voltage Noise vs Frequency**



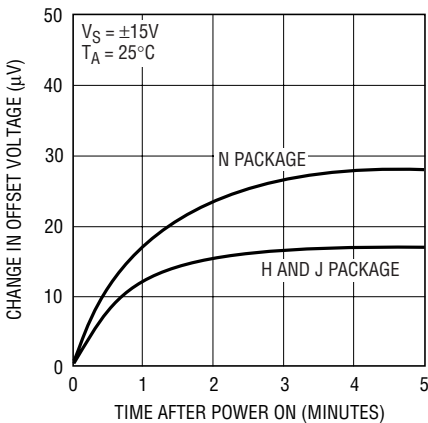
LT1102 • TPC12

**Input Bias Current Over the Common Mode Range**



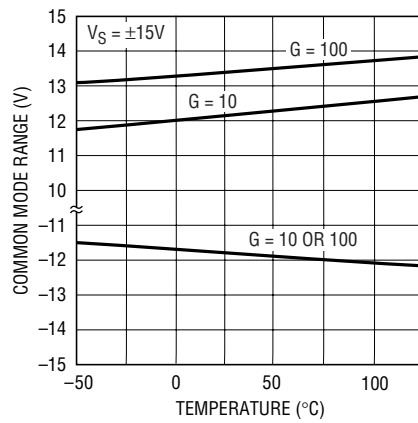
LT1102 • TPC13

**Warm-Up Drift**



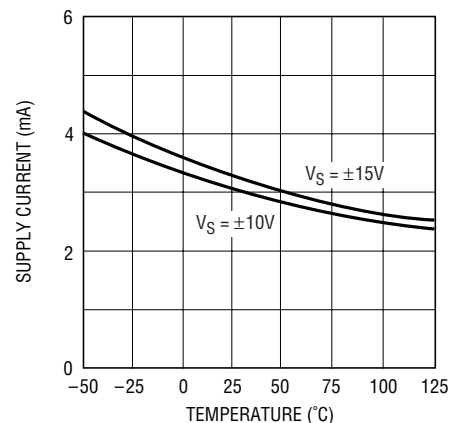
LT1102 • TPC14

**Common Mode Range vs Temperature**



LT1102 • TPC15

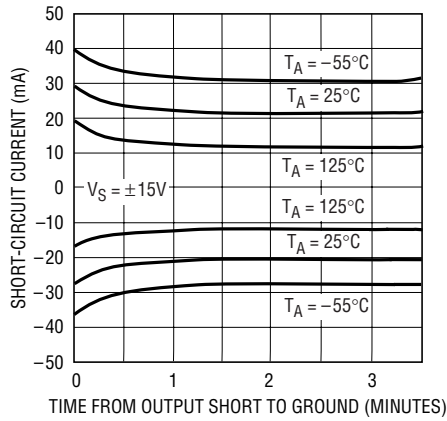
**Supply Current vs Temperature**



LT1102 • TPC16

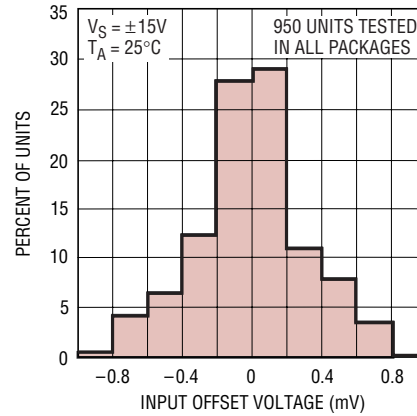
# TYPICAL PERFORMANCE CHARACTERISTICS

**Short-Circuit Current vs Time**



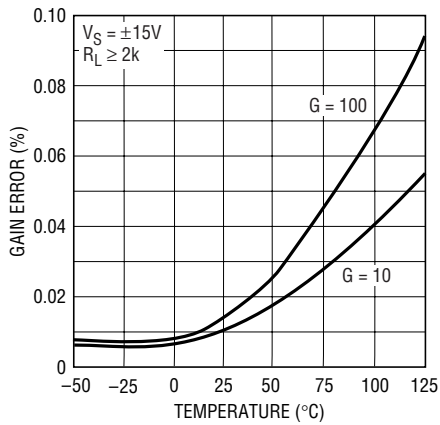
LT1102 • TPC17

**Distribution of Offset Voltage**



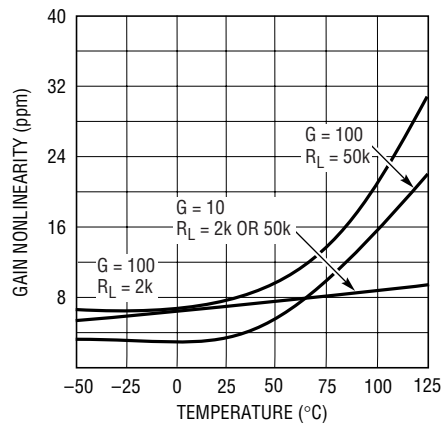
LT1102 • TPC18

**Gain Error vs Temperature**



LT1102 • TPC19

**Gain Nonlinearity Over Temperature**



LT1102 • TPC20

## APPLICATIONS INFORMATION

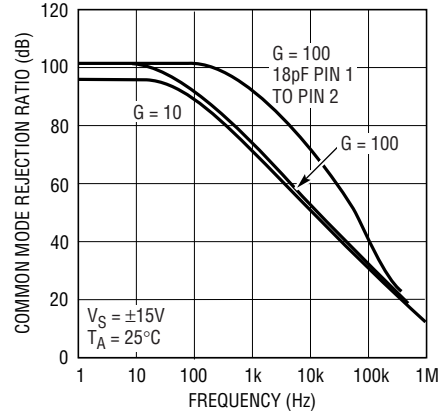
In the two op amp instrumentation amplifier configuration, the first amplifier is basically in unity gain, and the second amplifier provides all the voltage gain. In the LT1102, the second amplifier is decompensated for gain of 10 stability, therefore high slew rate and bandwidth are achieved. Common mode rejection versus frequency is also optimized in the  $G = 10$  mode, because the bandwidths of the two op amps are similar. When  $G = 100$ , this statement is no longer true; however, by connecting an 18pF capacitor between pins 1 and 2, a common mode AC gain is created to cancel the inherent roll-off. From 200Hz to 30kHz, CMRR versus frequency is improved by an order of magnitude.

### Input Protection

Instrumentation amplifiers are often used in harsh environments where overload conditions can occur. The LT1102 employs FET input transistors, consequently the differential input voltage can be  $\pm 30V$  (with  $\pm 15V$  supplies,  $\pm 36V$  with  $\pm 18V$  supplies). Some competitive instrumentation amplifiers have NPN inputs which are protected by back-to-back diodes. When the differential input Voltage exceeds  $\pm 13V$  on these competitive devices, input current increases to milliampere level; more than  $\pm 10V$  differential voltage can cause permanent damage.

When the LT1102 inputs are pulled below the negative supply or above the positive supply, the inputs will clamp a diode voltage below or above the supplies. No damage will occur if the input current is limited to 20mA.

**Common Mode Rejection Ratio vs Frequency**



LT1102 • A101

### Gains Between 10 and 100

Gains between 10 and 100 can be achieved by connecting two equal resistors ( $= R_X$ ) between pins 1 and 2 and pins 7 and 8.

$$\text{Gain} = 10 + \frac{R_X}{R + R_X/90}$$

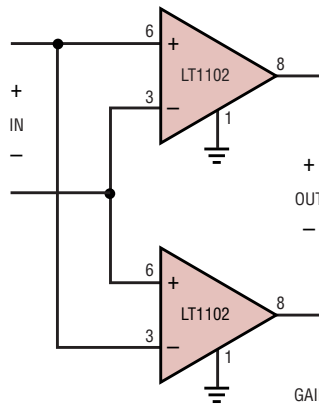
The nominal value of  $R$  is  $1.84k\Omega$ . The usefulness of this method is limited by the fact that  $R$  is not controlled to better than  $\pm 10\%$  absolute accuracy in production. However, on any specific unit, 90R can be measured between Pins 1 and 2.



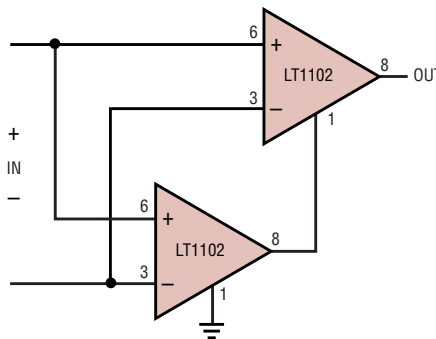
# APPLICATIONS INFORMATION

## Gain = 20, 110, or 200 Instrumentation Amplifiers

### Differential Output



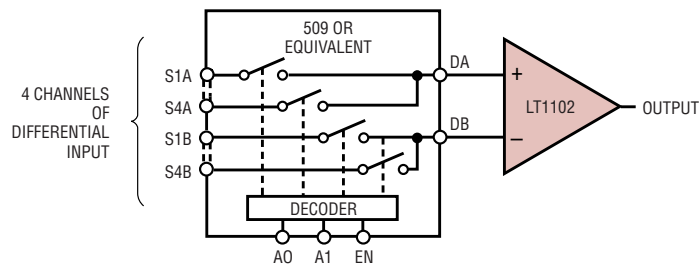
### Single Ended Output



GAIN = 200, AS SHOWN  
 GAIN = 20, SHORT PIN 1 TO PIN 2, PIN 7 TO PIN 8 ON BOTH DEVICES  
 GAIN = 110, SHORT PIN 1 TO PIN 2, PIN 7 TO PIN 8 ON ONE DEVICE,  
 NOT ON THE OTHER  
 INPUT REFERRED NOISE IS REDUCED BY  $\sqrt{2}$  (G = 200 OR 20)

LT1102 • AI02

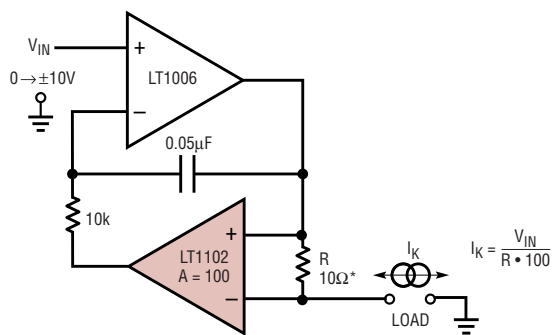
## Multiplexed Input Data Acquisition



800kHz SIGNALS CAN BE MULTIPLEXED WITH LT1102 IN G = 10

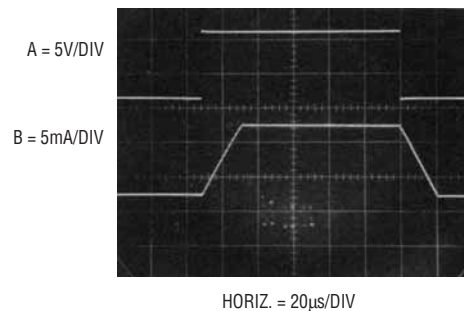
LT1102 • AI03

## Voltage Programmable Current Source is Simple and Precise



LT1102 • AI04

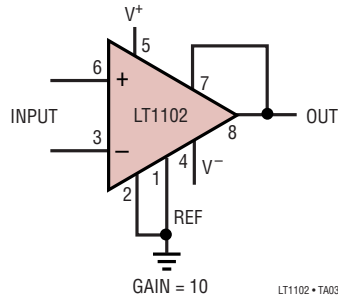
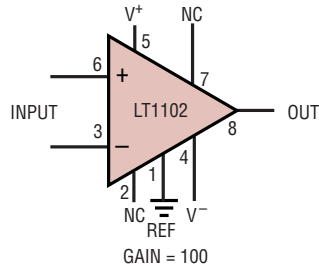
## Dynamic Response of the Current Source



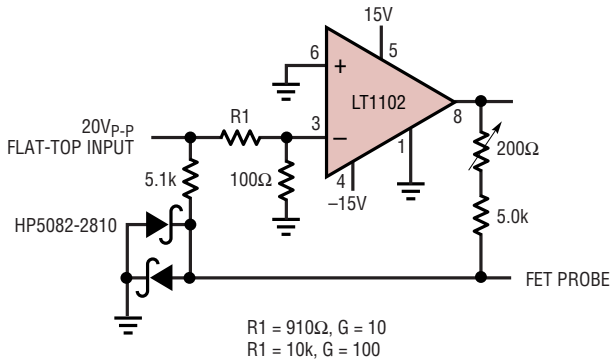
LT1102 • AI05

TYPICAL APPLICATIONS

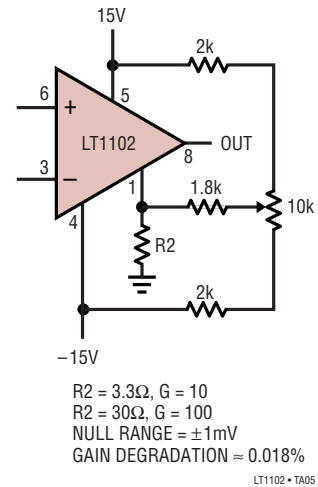
Basic Connections



Settling Time Test Circuit

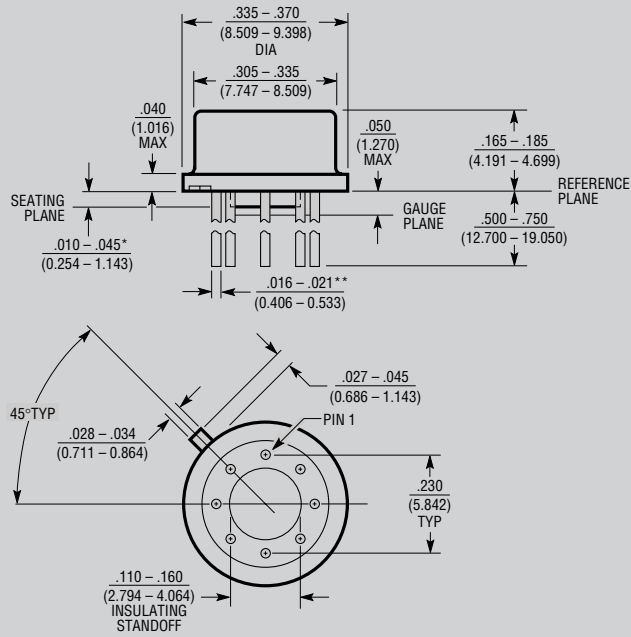


Offset Nulling



**PACKAGE DESCRIPTION**

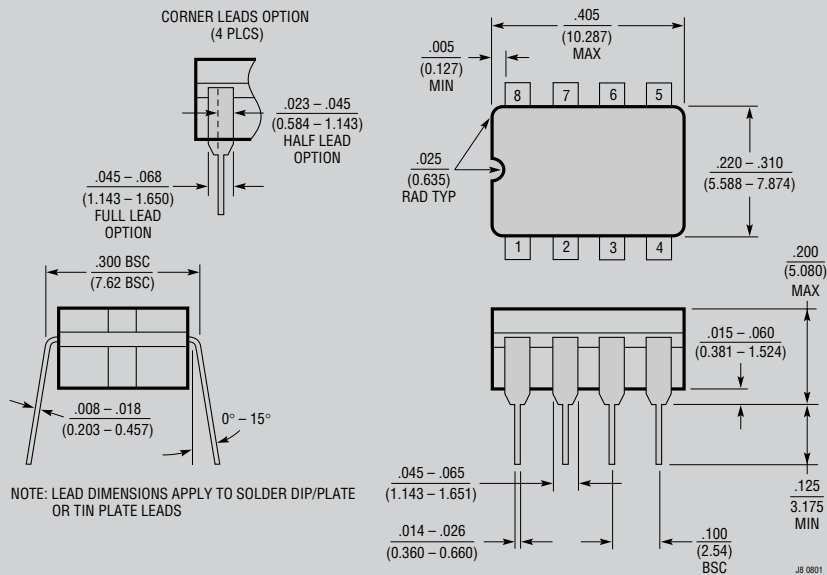
**H Package**  
**8-Lead TO-5 Metal Can (.230 Inch PCD)**  
 (Reference LTC DWG # 05-08-1321)



\* LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND THE SEATING PLANE

\*\* FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS .016 - .024 (0.406 - 0.610) H8 (TO-5) 0.230 PCD 0801

**J8 Package**  
**8-Lead Cerdip (Narrow .300 Inch, Hermetic)**  
 (Reference LTC DWG # 05-08-1110)



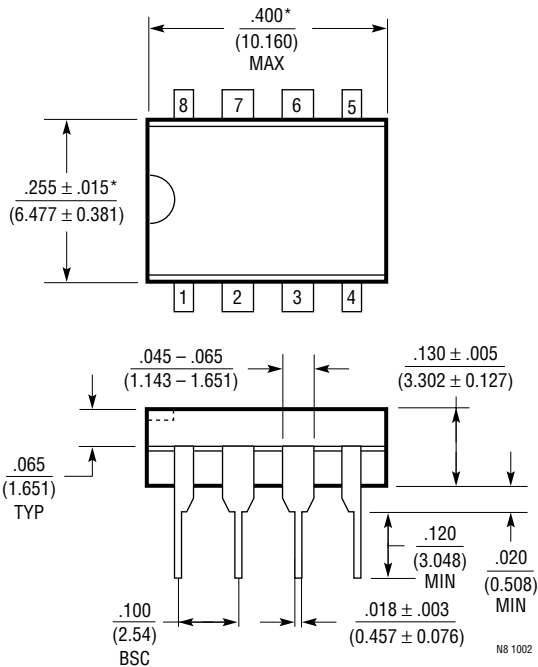
NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP/PLATE OR TIN PLATE LEADS

J8 0801

**OBSOLETE PACKAGES**

**PACKAGE DESCRIPTION**

**N8 Package**  
**8-Lead PDIP (Narrow .300 Inch)**  
 (Reference LTC DWG # 05-08-1510)



NOTE:  
 1. DIMENSIONS ARE  $\frac{\text{INCHES}}{\text{MILLIMETERS}}$   
 \*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.  
 MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)